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Dual-mode orthogonal Doherty power amplifier with efficiency enhancement and load mismatch adaptability

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Abstract: This study proposes an efficiency-enhanced dual-mode orthogonal Doherty power amplifier (ODPA) architecture. The operation theory, design process, and implementation of the proposed ODPA are introduced in detail. By introducing an orthogonal architecture with control signal power injection and incorporating a modified output matching network, the efficiency of Doherty power amplifiers under active load modulation can be enhanced. Furthermore, owing to the additional degrees of freedom provided by the orthogonal architecture, which enables independent amplitude and phase control and dynamic reshaping of the load modulation trajectories, and the dual-mode reciprocal bias configuration, the proposed ODPA exhibits high adaptability to load mismatch. To validate the proposed architecture, a 2.1-GHz dual-mode ODPA is designed and fabricated. With a matched load, the fabricated dual-mode ODPA exhibites over 60% drain efficiency throughout the power range from 6-dB output back-off (OBO) to saturation. For mismatched loads with a 2:1 voltage standing wave ratio, a saturated output power of 42.8–44.6 dBm and OBO efficiency of 47.2%–58.1% are obtained through mode reconfiguration.

Key words: Doherty power amplifier; Dual mode; High efficiency; Load mismatch; Orthogonal; Reciprocal bias

1 Introduction

Modern society faces an increasingly urgent energy crisis, making energy conservation one of the most pressing challenges for the future of humanity. As one of the most energy-intensive components in wireless communication systems, power amplifiers (PAs) must achieve high efficiency to support the vision of green communication. Modern communication systems typically use modulated signals with a high peak-to-average power ratio to improve spectrum utilization. This introduces significant design challenges for PAs, which must maintain high efficiency even in the output back-off (OBO) region.

To enhance efficiency in the OBO region, various PA architectures have been developed, including Doherty, outphasing, envelope tracking, and load-modulated balanced amplifiers. Among these, Doherty PAs (DPAs) stand out as one of the most widely adopted solutions for both base stations and user terminals owing to their simple circuit structure, mature design process, and high long-term reliability (Pang et al., 2015; Zheng et al., 2016; Zhou et al., 2017; Sun et al., 2021; Tang et al., 2023). Efficiency is the core performance metric of DPAs. By employing various high-efficiency operation modes (Colantonio et al., 2009; Zhang et al., 2020), the Doherty technique has achieved excellent efficiency performance in both the OBO and saturation regions. However, efficiency drop remains inevitable in the power range between the OBO and saturation regions due to the inherent load modulation characteristics of conventional DPAs. Although this issue has been partially addressed using techniques such as dual-input architectures (Barthwal et al., 2021; Shi et al., 2023; Xie et al., 2024), modified combining phases (Fang et al., 2018; Dai et al., 2024; Zeng et al., 2025), optimized turn-on time (Moon et al., 2011), and enhanced power distribution (Zheng et al., 2016), further improvements are required to maximize efficiency.

Recently, with the rapid advancement of wireless communication systems, the improvement of other performance metrics, such as bandwidth (Saad et al., 2019; Zhang et al., 2020) and linearity (Kang et al., 2017), has also become a major concern in PA design. In particular, performance insensitivity under load mismatch conditions becomes a new

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important indicator for PAs due to the difficulty of integrating isolators or circulators in the fifth-generation multiple-input multiple-output equipment with beamforming capabilities and the inevitable PA load change from mutual coupling between different antenna elements. To address this new load mismatch challenge, various techniques have been developed in recent years, such as reconfigurable output matching networks (OMNs) (Donahue et al., 2020), multiport active load pulling (Chappidi et al., 2020), dynamic supply voltage control (Gonçalves et al., 2022), digital Doherty operation (Hu et al., 2015), orthogonal load-modulated balanced amplifiers (Collins et al., 2020; Quaglia et al., 2022), and pseudo-Doherty architectures (Guo et al., 2025). Despite the mentioned efforts for PA efficiency and insensitivity enhancement, it is still difficult to achieve good back-off efficiency performance under load mismatch conditions.

In this study, we propose a modified DPA architecture, an orthogonal DPA (ODPA), to improve efficiency throughout the active load modulation range. This study is an extended version of the authors' previous conference paper (Gao et al., 2024), with the addition of more detailed theoretical analyses and circuit design specifics. The principle of ODPA is further analyzed using a nonlinear current source. Assistant input control signal power (CSP) and modified OMNs are used to modify Doherty load modulation, avoiding efficiency reduction between OBO and the peak power. The proposed ODPA architecture is also compatible with a dual-mode reciprocal bias configuration (Lyu and Chen, 2022; Han et al., 2024; Pang et al., 2024), which can improve the load insensitivity performance of DPAs by switching modes during load changes.

2 Theoretical analysis

2.1 ODPA operation

Fig. 1 shows the block diagram of the proposed ODPA architecture. Its physical circuit primarily comprises input and output couplers, carrier and peaking PAs with reciprocal gate bias, isolation port load, and two modified OMNs between transistors and output couplers. The proposed ODPA has a dual-input architecture, where the main radio frequency (RF) input and control signal are injected through the input and isolation port of the input coupler. Unlike most dual-input DPA systems, because of the presence of an input coupler, the proposed architecture achieves efficiency improvements even when the CSP is significantly lower than the main RF input power, thereby reducing the cost of additional control signal generation. Reciprocal gate bias technology is also introduced into the proposed ODPA architecture, which can resist several dynamic load mismatches using switchable isolated port loads. By switching different isolated port loads and the gate biases of the two sub-PAs, the proposed ODPA can operate in two modes. When the isolated port of the output coupler is grounded, the ODPA operates in mode I, with PA1 and PA2 functioning as the peaking and carrier PAs, respectively. Conversely, when the isolated port is open, the ODPA enters mode II, where PA1 and PA2 act as the carrier and peaking PAs, respectively.

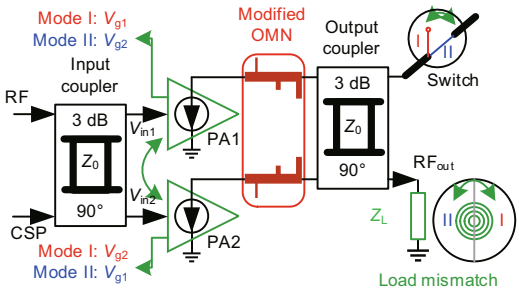

Fig. 1 Proposed dual-mode ODPA architecture. V_{g1} and V_{g2} are the gate bias voltages for PA1 and PA2, respectively. Z_L represents the practical load impedance terminated at the output port of the output coupler

To provide a clearer explanation of the operating principle of the proposed ODPA, the structure shown in Fig. 1 is simplified. This simplification considers a scenario without OMNs. A simplified block diagram is shown in Fig. 2. The impact of OMNs is further analyzed in a subsequent subsection. For the convenience of subsequent variable derivation, the amplitudes of the RF input and control signal voltages are denoted as $2V_{\mathrm{RFin}}$ and $2V_{\mathrm{CSPin}}\mathrm{e}^{\mathrm{j}\theta_0}$, respectively, where θ_0 denotes the phase offset between the control and RF input signals. When continuous wave signals with amplitudes $2V_{\mathrm{RFin}}$ and $2V_{\mathrm{CSPin}}\mathrm{e}^{\mathrm{j}\theta_0}$ are applied to the input and isolated ports of the input coupler, the resulting output voltages of the input coupler, V_{in1} and V_{in2}, can be described as follows:

$$\begin{cases} V_{\mathrm{in1}} = V_{\mathrm{RFin}} - \mathrm{j}V_{\mathrm{CSPin}}\mathrm{e}^{\mathrm{j}\theta_0}, \\ V_{\mathrm{in2}} = -\mathrm{j}V_{\mathrm{RFin}} + V_{\mathrm{CSPin}}\mathrm{e}^{\mathrm{j}\theta_0}. \end{cases} \tag{1}$$

The maximum input CSP is $\alpha V_{\mathrm{CSPin\_max}} = V_{\mathrm{RFin\_max}}$, where α denotes a scaling factor. The two separated input signals V_{in1} and V_{in2} are amplified by PA1 and PA2, respectively, and then output to the output coupler. PA1 and PA2 have different gate biases in different working modes and may work in Class C or AB. Therefore, the signal amplification process is also divided into two cases: carrier amplification (corresponding to Class B) and peaking amplification (corresponding to Class C). Only the carrier PA works when the normalized magnitude of V_{in} (which is V_{in1} in mode I and V_{in2} in mode II) is lower than β, and the peaking PA works when the normalized magnitude of V_{in} (which is V_{in2} in mode I and V_{in1} in mode II) is greater than β, where β represents the starting point of the peaking PA. The transconductance of both PAs is assumed to be 1 S (the derivation result is independent of

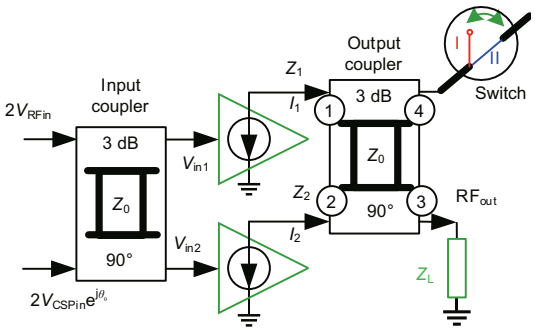

Fig. 2 Simplified theoretical block diagram of the proposed ODPA

the transconductance of the PAs). $V_{\text{in\_max}}$ denotes the input voltage that enables the transistor to obtain the maximum current output $I_{\max}$ when the load of the transistor is the optimal impedance R_{opt}.

$$I_{\text{Carrier}} = \frac{V_{\text{in}}}{V_{\text{in\_max}}} I_{\max}\ ,\ 0 \le \frac{|V_{\text{in}}|}{V_{\text{in\_max}}} \le 1, \tag{2}$$

$$I_{\text{Peaking}} = \begin{cases} 0\ , & 0 \le \dfrac{|V_{\text{in}}|}{V_{\text{in\_max}}} \le \beta, \\ \dfrac{V_{\text{in}}}{|V_{\text{in}}|V_{\text{in\_max}}} \dfrac{|V_{\text{in}}| - \beta}{1-\beta}\ ,\ & \beta < \dfrac{|V_{\text{in}}|}{V_{\text{in\_max}}} \le 1, \end{cases} \tag{3}$$

where I_{Carrier} represents the current of the carrier power amplifier at the current-source terminal, and I_{Peaking} refers to the current of the peaking amplifier at the current-source terminal.

After the addition of the CSP, V_{in1} and V_{in2} may be out of the range of 0–$V_{\text{in\_max}}$, and the excess will not be considered. Therefore, the input of the active devices can be limited to 0–$V_{\text{in\_max}}$. Using the $\boldsymbol{Z}$ matrix of the coupler, the relationship between the voltage V_i and current I_i ($i = 1, 2, 3, 4$) at the four ports of the coupler can be expressed as follows:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & -\mathrm{j} & -\mathrm{j}\sqrt{2} & 0 \\ -\mathrm{j} & 0 & 0 & -\mathrm{j}\sqrt{2} \\ -\mathrm{j}\sqrt{2} & 0 & 0 & -\mathrm{j} \\ 0 & -\mathrm{j}\sqrt{2} & -\mathrm{j} & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}, \tag{4}$$

where Z_0 denotes the characteristic impedance of the output coupler. For ODPA mode I, PA1 and PA2 function as the peaking and carrier PAs, respectively. When the load of the ODPA is set to Z_0, the current configuration can be expressed as follows:

$$\begin{cases} I_1 = I_{\text{Peaking}}, \\ I_2 = I_{\text{Carrier}}, \\ I_3 = \dfrac{V_3}{Z_0}, \\ I_4 = \dfrac{V_4}{\mathrm{j}X}. \end{cases} \tag{5}$$

By substituting Eq. (5) into Eq. (4), the impedance of the two input ports Z_1 and Z_2 of the output coupler can be obtained as follows:

$$\begin{cases} Z_1 = -\mathrm{j}Z_0 \left(\dfrac{I_2}{I_1} + \dfrac{\mathrm{j}2 + \frac{2Z_0}{\mathrm{j}X}\frac{I_2}{I_1}}{1 - \frac{Z_0}{\mathrm{j}X}} \right), \\ Z_2 = \mathrm{j}Z_0 \left(\dfrac{I_1}{I_2} + \dfrac{\mathrm{j}\frac{2I_1}{I_2} + \frac{2Z_0}{\mathrm{j}X}}{1 - \frac{Z_0}{\mathrm{j}X}} \right). \end{cases} \tag{6}$$

The load of the sub-PAs is determined by the output currents I_1 and I_2 and the isolated port load $\mathrm{j}X$. Note that I_1 and I_2 contain the amplitude and phase information of the output current. As a typical case, when the isolated port of the output coupler is short-circuited to ground, that is, $\mathrm{j}X = 0$, Z_1 and Z_2 can be simplified to the following equation:

$$\begin{cases} Z_1 = \mathrm{j}Z_0 \dfrac{I_2}{I_1}, \\ Z_2 = \mathrm{j}Z_0 \left(\dfrac{I_1}{I_2} - \mathrm{j}2 \right). \end{cases} \tag{7}$$

Similarly, for ODPA mode II, the carrier amplifier and the peaking amplifier are swapped, and the current configuration can be expressed as

$$\begin{cases} I_1 = I_{\text{Carrier}}, \\ I_2 = I_{\text{Peaking}}, \\ I_3 = \dfrac{V_3}{Z_0}, \\ I_4 = \dfrac{V_4}{\mathrm{j}X}. \end{cases} \tag{8}$$

As a typical case, when the isolated port of the output coupler is open, that is, $\mathrm{j}X = \infty$, Z_1 and Z_2 can be simplified to the following equation:

$$\begin{cases} Z_1 = -\mathrm{j}Z_0 \left(\dfrac{I_2}{I_1} + \mathrm{j}2 \right), \\ Z_2 = -\mathrm{j}Z_0 \dfrac{I_1}{I_2}. \end{cases} \tag{9}$$

Thus far, the active load modulation impedances of the carrier and peaking PAs can be determined. Fig. 3 illustrates these active load modulation impedances in mode I on a Smith chart using a normalized reference impedance of R_{opt}. The isolated port of the output coupler is short-circuited to ground. The normalized amplitude of V_{RFin} is varied from 0.4 to 1.0 in increments of 0.05, with V_{CSPin} amplitude fixed at 0.1, and the phase θ_0 scanned from 0° to 360° in 10° steps. Both sub-PAs have the same $I_{\max}$. The turn-on point of the peaking PA β is set to 0.5. For comparison, the colored lines on the real axis of the Smith charts represent the load modulation curves when there is no control signal input into the ODPA, that is, a single RF input. The inclusion of the control signal allows the active load modulation process to cover a wider impedance range. This extension enables the ODPA to maintain optimal impedance conditions across the OBO range or during load mismatch, supporting high-efficiency operation. Notably, in mode II, if the isolation port is set to an open circuit, the load modulation impedance results of the carrier and peaking PAs will be the same as those in mode I.

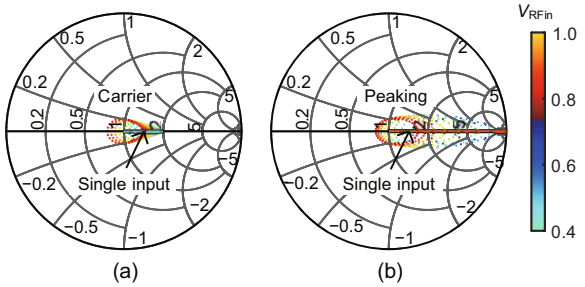

Fig. 3 Active load modulation impedance of carrier PA (a) and peaking PA (b)

2.2 Nonlinear current source analysis

In the previous analysis, the impedance modulation relationship of the coupler port was obtained, and the impedance active load modulation data of the simplified dual-input ODPA were obtained under the assumption of linear amplification in Eqs. (2) and (3). These analyses are all based on the sub-PAs operating in standard Class B conditions. However, when considering the addition of OMN $\mathrm{j}X$ and the load mismatch conditions, the assumption of linear current has shown its

limitations. The load of the sub-PAs will be much more complicated and in many cases it will no longer operate in Class B. Therefore, the predicted results will deviate significantly from the actual circuit.

To make the theoretical derivation results closer to the actual circuit, a nonlinear current source (Chen et al., 2022; Pang et al., 2024) is introduced here for further analysis. For a field effect transistor (FET), its drain current $I_{\mathrm{ds,non}}$ can be approximated by Eqs. (10) and (11):

$$I_{\mathrm{ds,non}} = I_{\max}\psi\left(v_{\mathrm{gs}}\right)\tanh\left(v_{\mathrm{ds}}/v_{\mathrm{knee}}\right), \tag{10}$$

$$\psi(x) = \begin{cases} 1, & x > 1, \\ x, & 0 \le x \le 1, \\ 0, & x < 0. \end{cases} \tag{11}$$

Here, v_{ds}, v_{gs}, and v_{knee} represent the drain-to-source, gate-to-source, and knee voltages of the FET, respectively. After adopting the assumption of nonlinear current, the output currents of the carrier PA $I_{\mathrm{c,non}}$ and the peaking PA $I_{\mathrm{p,non}}$ can be rewritten as

$$I_{\mathrm{c,non}} = I_{\mathrm{ds,non}}\big|_{v_{\mathrm{gs}}=V_{\mathrm{in}}}, \tag{12}$$

$$I_{\mathrm{p,non}} = \begin{cases} 0, & 0 \le \dfrac{|V_{\mathrm{in}}|}{V_{\mathrm{in\_max}}} \le \beta, \\ I_{\mathrm{ds,non}}\big|_{v_{\mathrm{gs}}=\frac{V_{\mathrm{in}}}{|V_{\mathrm{in}}|V_{\mathrm{in\_max}}}\frac{|V_{\mathrm{in}}|-\beta}{1-\beta}}, & \beta < \dfrac{|V_{\mathrm{in}}|}{V_{\mathrm{in\_max}}} \le 1. \end{cases} \tag{13}$$

Compared with the linear current assumption, the nonlinear current assumption not only considers the knee voltage of the transistor, but also includes the characteristics of the transistor when overdriven, enabling the characteristics of the transistor under various load and input conditions to be characterized more precisely. In the following analysis, $I_{\max}$ = 2 A, v_{knee} = 2 V, and the drain DC supply of the transistor equals 30 V. In addition, the impact of OMNs is considered in the following analysis. To achieve matching between two complex impedances, the OMN can be equivalent to the network shown in Fig. 4, where the Transformer completes the pure impedance conversion, and θ_{OMN} matches the imaginary impedance and provides the phase information for the OMN. The characteristic impedance of the output coupler is set to 50 Ω for compatibility with most commercial couplers. Therefore, based on Eqs. (7) and (9), when the PA is saturated, the OMN needs to achieve the matching from R_{opt} to 50 Ω. This can determine the parameters of the Transformer responsible for the real-part matching in the OMN equivalent network, and the value of the equivalent phase θ_{OMN} can further determine the impedance matched by the OMN at the OBO point, along with the coupler port OBO impedance determined by Eq. (6). As shown in Fig. 4, an open transmission line (OTL) with a characteristic impedance of 50 Ω and a phase of θ_{iso} can be used to provide a load jX for the isolated port. In the proposed ODPA architecture, it can be proved that as long as θ_{OMN} and θ_{iso} satisfy a specific relationship, the OBO state can be matched by the OMN, and the DPA working mode can be realized. $Z_{1\mathrm{t}}$ is the equivalent load impedance of PA1 at the current source terminal. $Z_{2\mathrm{t}}$ is the equivalent load impedance

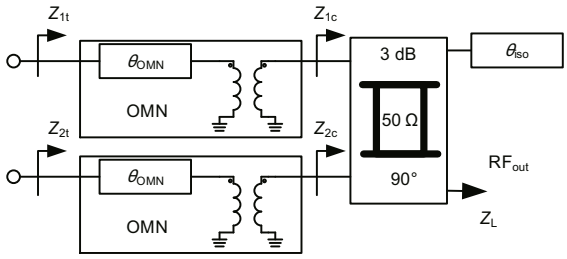

Fig. 4 Equivalent network of the OMN in ODPA

of PA2 at the current source terminal. $Z_{1\mathrm{c}}$ is the equivalent load impedance of PA1 at the input port of the coupler. $Z_{2\mathrm{c}}$ is the equivalent load impedance of PA2 at the coupler's coupled port.

First, consider the case of a single RF input, that is, when there is no control signal. Fig. 5 shows the load variation of the coupler port and transistor port of ODPA with input power when θ_{OMN} changes from 0° to 90° with a step of 15°. The reference impedance of the Smith chart is set to R_{opt}. θ_{OMN} and θ_{iso} satisfy the following relationship:

$$\theta_{\mathrm{iso}} = 90^\circ - \theta_{\mathrm{OMN}}. \tag{14}$$

It can be seen from Figs. 5a and 5b that when θ_{OMN} and θ_{iso} satisfy the relationship in Eq. (14), the load modulation impedance of the coupler port will change with the change of θ_{OMN}. Since we have determined the parameters for the Transformer in the OMN equivalent network, the impedance at the saturation point remains unchanged. On the other hand, the transistor port load in Figs. 5c and 5d can be fully compensated by the OMN and the isolation port load to the real axis to achieve the DPA load modulation effect. Similar results can be obtained in mode II. In fact, when the load of ODPA is a matched load, that is, 50 Ω, many characteristics of mode I and mode II are basically the same. The difference between the two modes will appear only when the load is mismatched. Therefore, in the following analysis, we analyze only the situation of mode I. The results obtained are also applicable to mode II after a simple conversion.

Fig. 6 shows the theoretical drain efficiency (DE) and output power obtained after adding the control signal under the assumption of nonlinear current. OMN uses the equivalent network mentioned in the previous analysis, and the Transformer achieves the real-part matching of 50 Ω to R_{opt}, while θ_{OMN} can take any value as analyzed before; only θ_{iso} needs to be adjusted accordingly to obtain the correct modulation result. The maximum input power of the CSP is set to be 10 dB lower than the maximum power of the main RF input, and θ_0 is swept in the range of 0°–360° with a step of 20°. It can be seen from Fig. 6 that although the CSP is added, the efficiency of the PA is almost not improved compared with the case when the CSP is off. This shows that simply introducing dual-input configuration under the traditional output matching strategy cannot improve the performance of the PA. Fig. 7 shows the load modulation impedance of the carrier PA and the peaking PA after adding the CSP in the Smith chart. Compared with Fig. 3, the difference between the analysis results obtained by the linear current assumption and the nonlinear current assumption can be clearly seen. Fig. 3 can analyze only the results of the PA working in normal Class B conditions, while

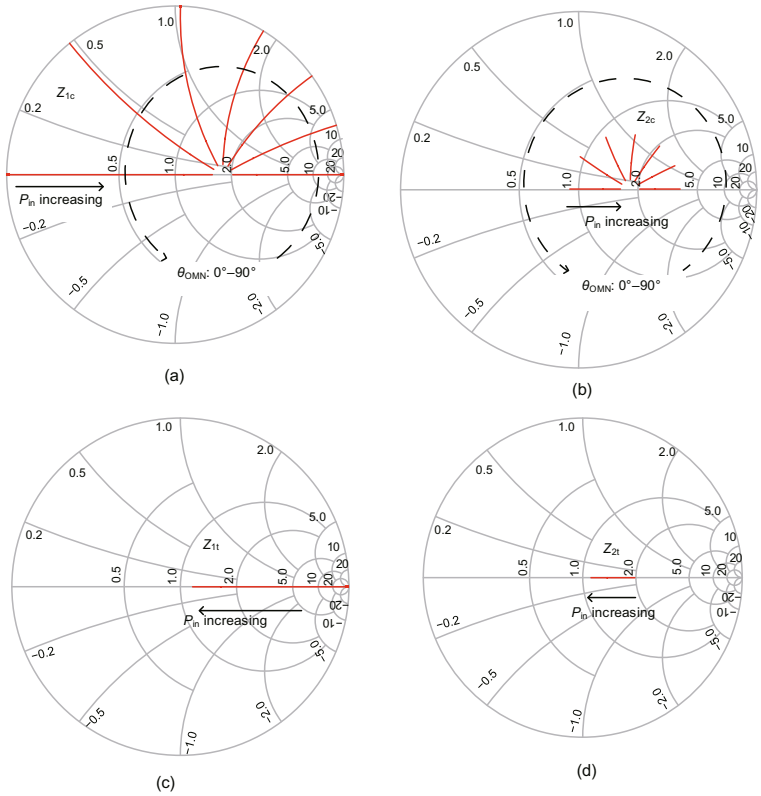

Fig. 5 Mode I load modulation impedance with different θ_{OMN} values in the Smith chart with reference impedance R_{opt}: (a) $Z_{1\mathrm{c}}$; (b) $Z_{2\mathrm{c}}$; (c) $Z_{1\mathrm{t}}$; (d) $Z_{2\mathrm{t}}$

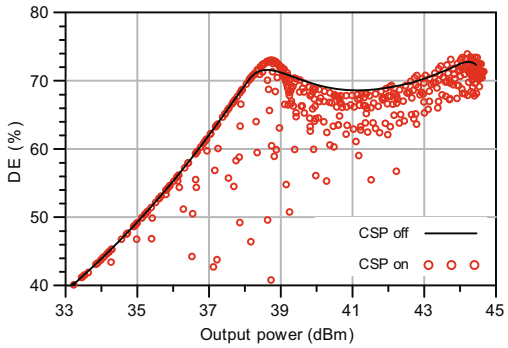

Fig. 6 Theoretical efficiency and output power after adding a control signal when using traditional OMN

the results obtained by using the nonlinear current assumption can be regarded as a supplement to the analysis under the linear current assumption. In addition to the ideal Class B situation, the PA can be analyzed in non-Class B situations such as overdrive and mismatch.

To further improve the efficiency of the PA and better use the flexibility brought by the dual-input configuration, a modified OMN structure is introduced in the ODPA, and its equivalent network is shown in Fig. 8. In the modified OMN, a series reactance $\mathrm{j}X_{\mathrm{OMN}}$ is additionally added based on the traditional OMN. By adding a suitable reactance $\mathrm{j}X_{\mathrm{OMN}}$, the load modulation in the dual-input configuration can be adjusted, thereby improving efficiency.

Fig. 9 shows the theoretical DE and output power obtained after the addition of the control signal and modified OMN under the assumption of nonlinear current. The additional series reactance $\mathrm{j}X_{\mathrm{OMN}}$ is set to j7.5 Ω by selecting the optimal efficiency performance. The maximum input power of the CSP is set to be 10 dB lower than the maximum power of the main RF input, and θ_0 is swept in the range of 0°–360° with a step of 20°. As shown in Fig. 9, after the incorporation of the modified OMN and control signal, the efficiency of the supplier is significantly improved compared with the single-input case, and the overall efficiency of the PA in the entire back-off range is enhanced. The maximum efficiency improvement reached 5 percentage points (PPs), and the saturated output power also increased by 0.8 dB. Fig. 10 shows the load modulation impedance of the carrier and peaking PAs after the incorporation of the CSP and modified OMN in the Smith chart. A comparison of Figs. 7 and 10 illustrates the impact of the modified OMN on load modulation in the dual-input case. Notably, in addition to the impact of the fundamental impedance, the impact of the additional series reactance $\mathrm{j}X_{\mathrm{OMN}}$ on the harmonic impedance is a reason for achieving efficiency improvement.

From the above analysis, it can be concluded that by adding a series reactance $\mathrm{j}X_{\mathrm{OMN}}$ to the OMN and cooperating with the CSP, the ODPA can achieve an improvement in efficiency within the OBO range and an increase in saturated output power. The performance of the proposed ODPA under load mismatch conditions will be analyzed in the next section.

3 Circuit design

To verify the previous analysis of the proposed ODPA architecture, a dual-mode ODPA using commercial GaN

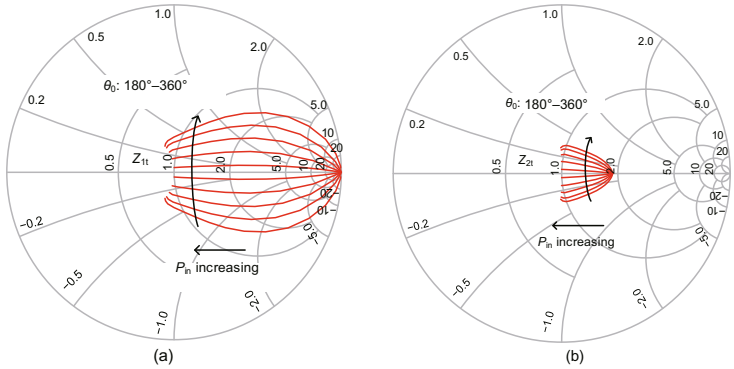

Fig. 7 Load modulation impedance with CSP in the Smith chart with reference impedance R_{opt}: (a) Z_{1t}; (b) Z_{2t}

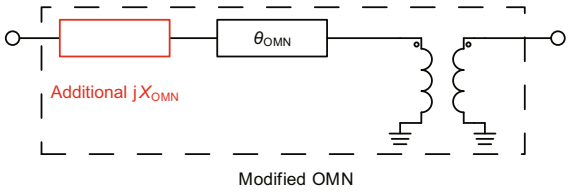

Fig. 8 Modified OMN equivalent network

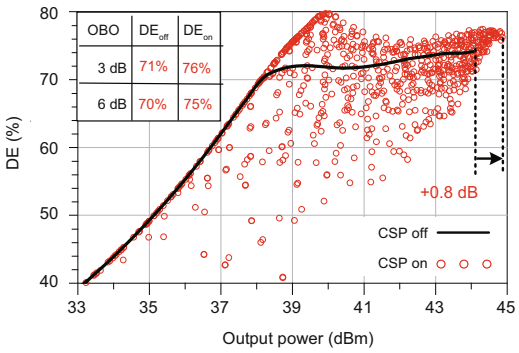

Fig. 9 Theoretical efficiency and output power after adding a control signal when using modified OMN

transistors was designed and fabricated at 2.1 GHz. GaN high electron mobility transistors (HEMTs) (CG2H40010F) from Wolfspeed were used as the active devices. The design was implemented on RO4350b substrate with a relative dielectric constant of 3.66. The design of ODPA is relatively simple due to its symmetry, and mainly includes four parts: input/output coupler, input matching network, OMN, and isolation port load. Two identical 3-dB one-order branch line couplers with a characteristic impedance of 50 Ω were used as the input and output couplers in this design. Fig. 11 shows the simulation results of relevant parameters of the designed coupler. It can be seen that the designed coupler has an insertion loss and coupling of nearly 3.2 dB at the operating frequency of 2.1 GHz, and the return loss and isolation are both lower than 30 dB, which will ensure the correct operation of the ODPA. The input matching is achieved by a T-shaped network, and the matching impedance is determined based on the source-pull data. In addition, a gate resistor and a resistor–capacitor stabilization circuit (RC) parallel network were added to improve the stability of the circuit. Two identical input matching networks were used to ensure phase consistency between the two sub-PAs regardless of the input matching networks.

According to the previous analysis, the modified OMN needs to achieve matching from the characteristic impedance of the output coupler, which is 50 Ω to the transistor R_{opt}, and add an additional series reactance jX_{OMN} on this basis. R_{opt} of the transistor CG2H40010F is about 30 Ω. At the same time, the influence of the parasitic network inherent in the transistor itself also needs to be considered. By integrating the parasitic network of the transistor into the OMN design, the parasitic network can be set as a part of the OMN to obtain the desired matching effect. Fig. 12 shows the schematic of the modified OMN, together with an equivalent parasitic network of CG2H40010F. As shown in Fig. 12, to achieve good matching and facilitate the adjustment of harmonic impedance, the OMN designed this time adopts a high-order series–parallel microstrip line structure for matching. In addition, the phase characteristics of the OMN need to be paid attention to. As mentioned in the previous analysis, the phase of the OMN will determine the load of the isolation port of the output coupler. The phase of the OMN designed in this paper is 90° at the operating frequency.

Fig. 13 shows the matched fundamental, second-harmonic and third-harmonic impedance of the designed OMN (including the equivalent parasitic network) when the load is 50 Ω. The reference impedance of the Smith chart is 30 Ω, which equals R_{opt}. It can be seen that the fundamental impedance matched by the OMN is connected in series with an additional reactance on the basis of R_{opt}, which slightly deviates from the center of the Smith chart. The value of the reactance is adjusted and selected according to the simulation performance. In this design, the value is set to be j12 Ω. Like the input matching network, two symmetrical OMNs are adopted to better support dual-mode reciprocal bias configuration. The load of the output coupler isolation port is realized by an OTL with a characteristic impedance of 50 Ω. The phase of the OTL is determined by the phase of the OMN. However, in the actual design process, the value of the isolation port load impedance can be adjusted and optimized according to the simulation situation to achieve optimal performance. In mode I, the isolated port is terminated with an OTL with an electrical length of 65°. And in mode II, the electrical length of the OTL is 159°. The length of the OTL can be switched by soldering RF short-circuit capacitor on the printed circuit board (PCB). Here, when PA1 is working as a peaking PA, it is defined as

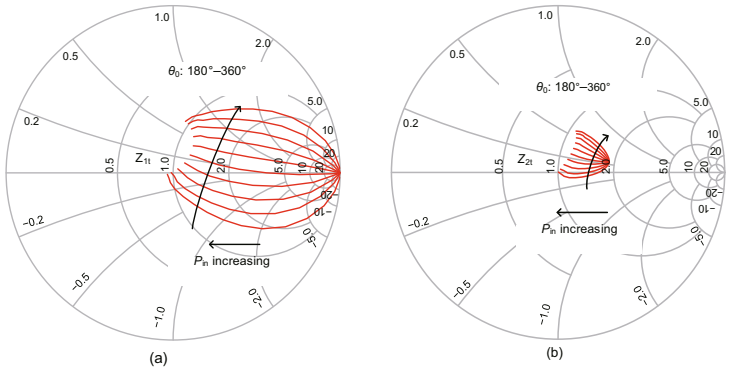

Fig. 10 Load modulation impedance with CSP and modified OMN in the Smith chart with reference impedance R_{opt}: (a) Z_{1t}; (b) Z_{2t}

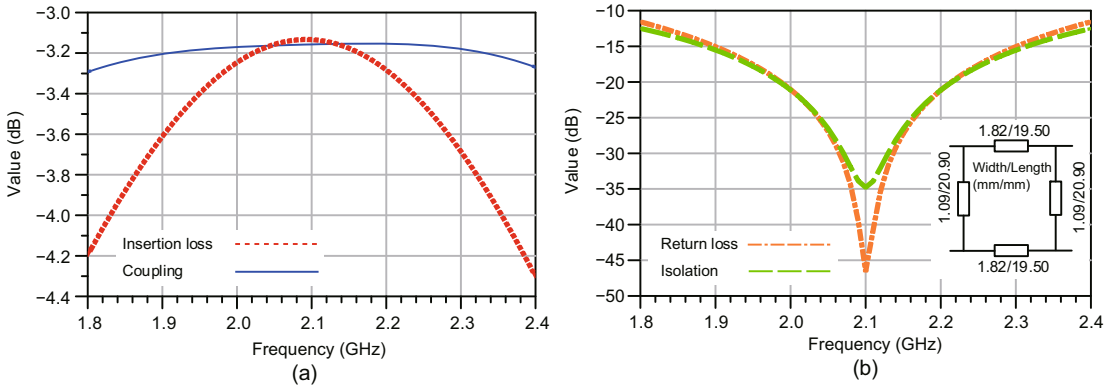

Fig. 11 Input/output coupler simulation: (a) insertion loss and coupling; (b) return loss and isolation

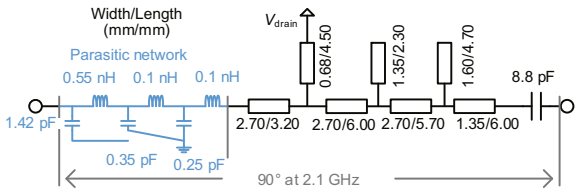

Fig. 12 Schematic of the modified OMN

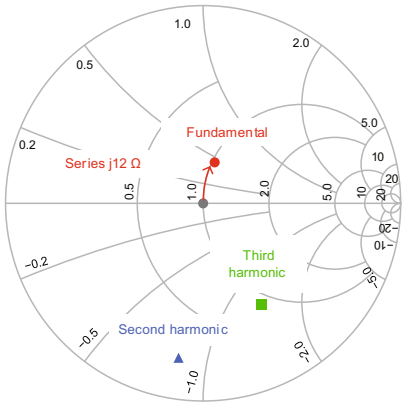

Fig. 13 Matched fundamental and harmonic impedance of the modified OMN with a load of 50 Ω

mode I, and when PA1 is working as a carrier PA, it is defined as mode II. Due to the influence of the OMN phase on the isolated port load, the isolated port load is no longer suitable as a criterion for distinguishing the two working modes.

Fig. 14 shows a schematic of the proposed ODPA with detailed dimensions. Fig. 15 shows the DE versus output power under a 50-Ω load at 2.1 GHz. For comparison, the single-input case without the control signal is also plotted in the figure. During the process, the gate bias voltages of the carrier and peaking PAs were set to −2.9 and −4.5 V, respectively. The drain supply voltage was set to 28 V. The maximum power of the main RF input signal was set to 33 dBm, and the CSP was constant at 20 dBm, which is 13 dB lower than the maximum main RF input power. The phase of the control signal is swept from 0° to 360° in steps of 10°. In mode I, after the addition of the control signal, the DE of the designed ODPA increased by up to 9 PPs within the OBO range, and the saturated output power increased by 0.8 dB (Fig. 15a). The saturated output power is 45.2 dBm with a DE of 75.6%. The DE at 6-dB OBO is 71%. In mode II, after the addition of the control signal, the DE of the designed ODPA increased by up to 15 PPs within the OBO range, and the saturated output power increased by 0.5 dB (Fig. 15b). The saturated output power is 45.5 dBm with a DE of 73.4%. The DE at 6-dB OBO is 72%. Based on the optimal efficiency contours, the gain versus output power curves were extracted (Fig. 16). In both modes, the small-signal gain is approximately 15 dB, whereas the saturated gain is approximately 10 dB.

The operation of the designed ODPA under load mismatch condition is also simulated. Figs. 17 and 18 show the relationship between the simulated DE and output power of the designed ODPA in mode I and mode II respectively, when the load mismatch voltage standing wave ratio (VSWR) is

2:1. Six different load impedances are selected to test the performance of the ODPA under mismatch conditions, and the load impedances are marked in the Smith chart in each sub-figure. The load impedances in sub-figures (a) through (f) correspond to VSWR phases ranging from −60° to 240°, in 60° increments. The other circuit parameters remain unchanged during the simulations, and the CSP is constant at 20 dBm. It can be seen from the simulation that no matter it is in mode I or mode II, the designed ODPA can show good efficiency in the entire OBO range under some specific load mismatch conditions, while in all other cases the OBO efficiency will be significantly reduced. For example, in mode I, Figs. 17a–17d, and in mode II, Fig. 18a and Figs. 18d–18f all show good OBO efficiency performance. Both mode I and mode II show complementary characteristics for different load mismatch conditions.

Fig. 19 provides a more specific and intuitive description of this complementary feature. Fig. 19a shows the 6-dB OBO

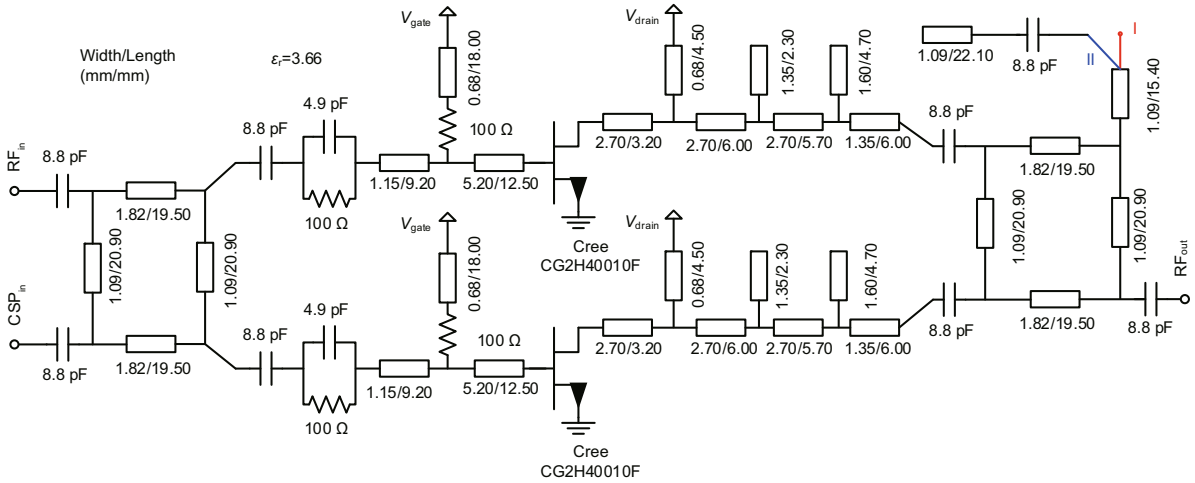

Fig. 14 Schematic of the proposed ODPA

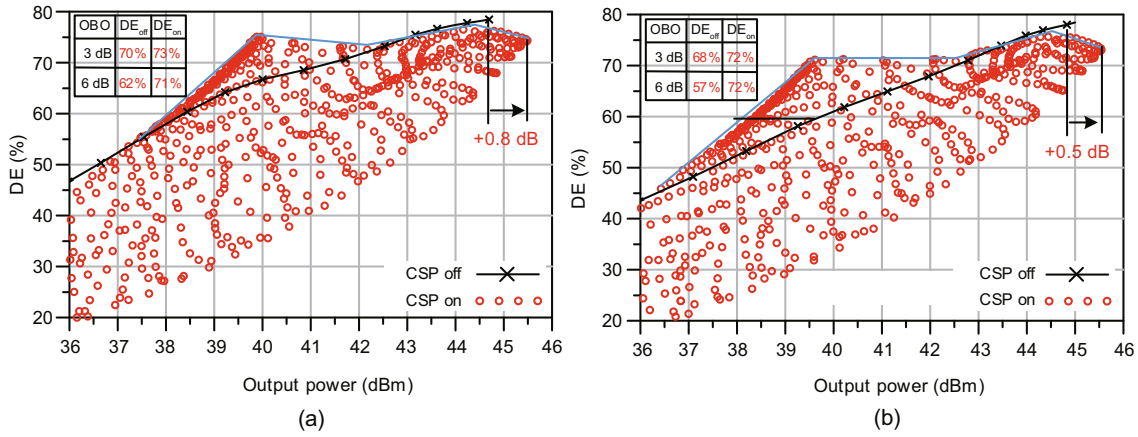

Fig. 15 Simulated DE versus output power at 2.1 GHz: (a) mode I; (b) mode II

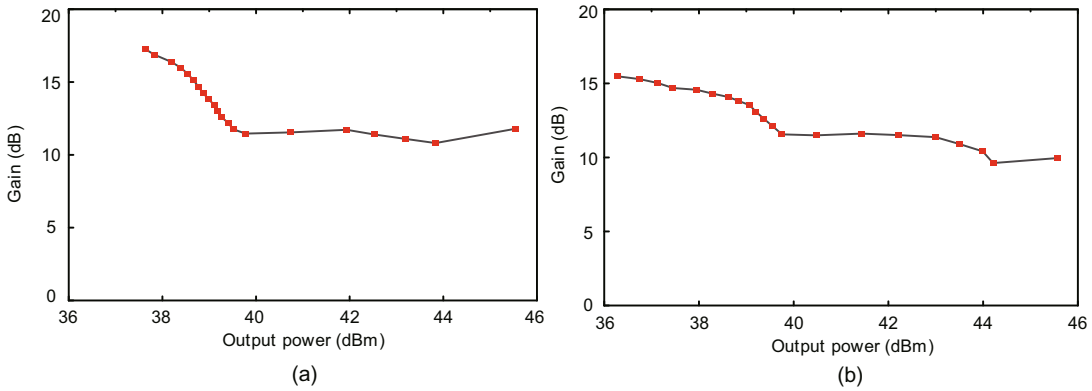

Fig. 16 Simulated gain versus output power at 2.1 GHz: (a) mode I; (b) mode II

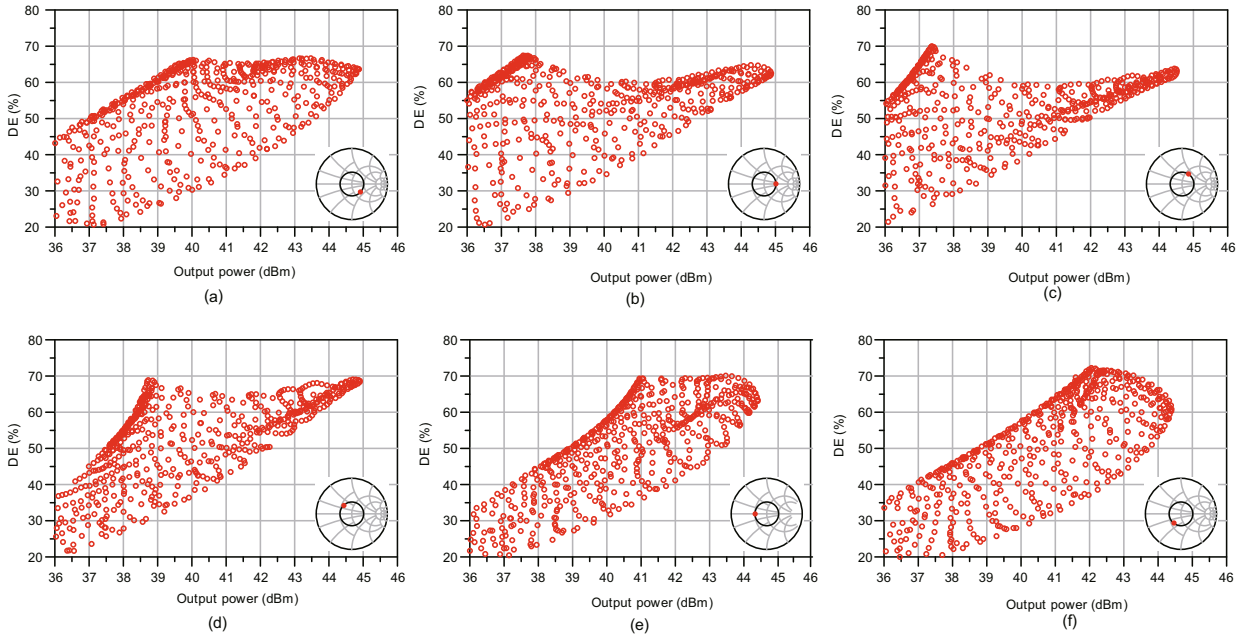

Fig. 17 Simulated DE versus output power under 2:1 VSWR in mode I: (a) −60°; (b) 0°; (c) 60°; (d) 120°; (e) 180°; (f) 240°

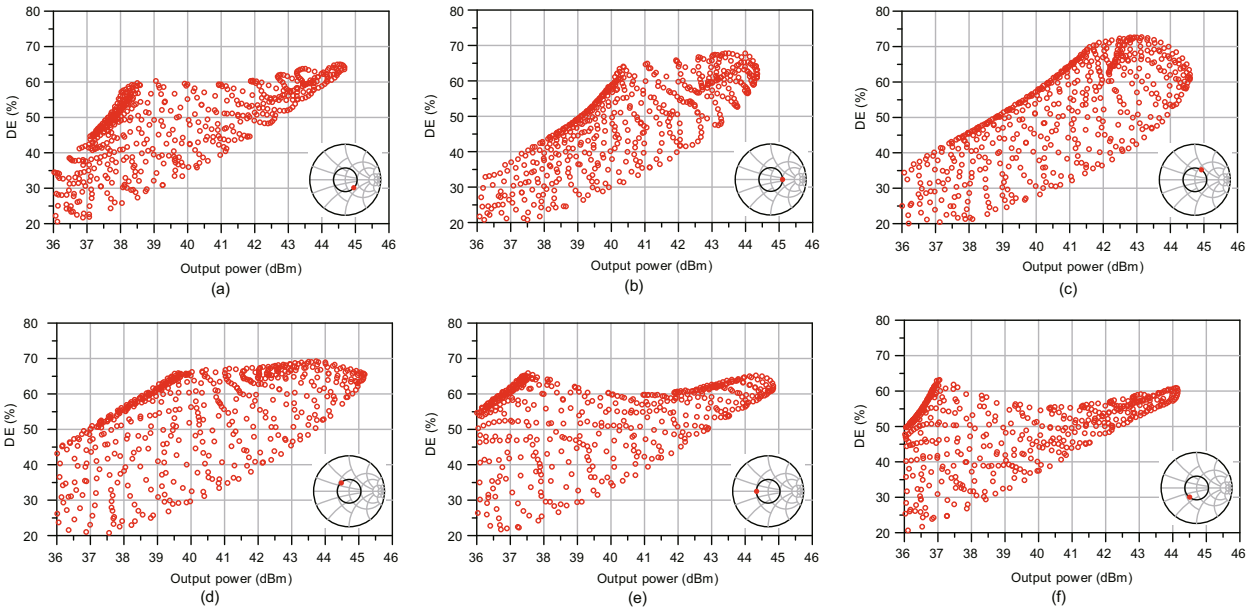

Fig. 18 Simulated DE versus output power under 2:1 VSWR in mode II: (a) −60°; (b) 0°; (c) 60°; (d) 120°; (e) 180°; (f) 240°

DE, while Fig. 19b shows the saturated DE and output power of the two modes under different mismatch load conditions. The 6-dB OBO here means backing off 6 dB from the maximum output power of each individual state. It can be seen intuitively that when the phase of VSWR is in the range of −60° to 120°, mode I has better OBO efficiency, while when the phase of VSWR is in the range of 120° to 240°, mode II performs better. The saturation efficiency and output power of the two modes are not significantly different. By combining the two modes, the designed ODPA can achieve a 6-dB OBO DE higher than 58.7% and saturated output power greater than 44.2 dBm under all load mismatch conditions with a VSWR of 2:1 in the simulations. Compared to the case of a 50-Ω load, the saturated output power is reduced by only 1.3 dB at most.

4 Measurement results

Fig. 20 shows a photo of the fabricated ODPA, a circuit used to provide a mismatched load for testing. The mismatched load test circuit first matches the 50-Ω load to 100 Ω, and then uses microstrip lines with a 50-Ω characteristic impedance of different phases to match the impedance to six different positions on the 2:1 VSWR circle in the Smith chart. Different load mismatch states are provided to the ODPA by

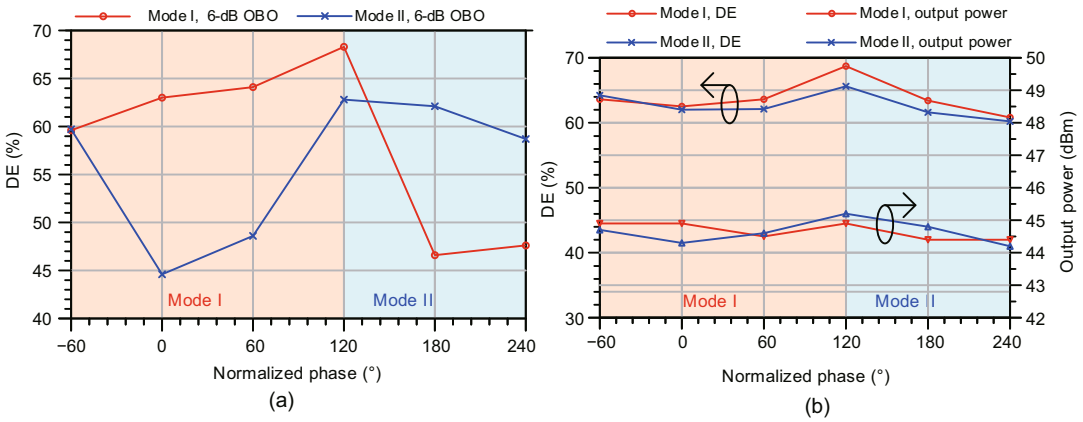

Fig. 19 Simulations under 2:1 VSWR over the entire phase range: (a) DE at 6-dB OBO; (b) DE and output power at saturation

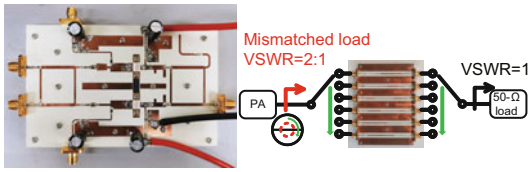

Fig. 20 Photograph of the fabricated ODPA and mismatched load test circuit

switching different circuit channels.

During the test, the drain quiescent current of the carrier PA was controlled at 50 mA, while the gate bias voltage of the peaking PA was −4.5 V. The drain supply voltage of both sub-PAs was set to 28 V. When there is no control signal input, the corresponding port of the input coupler is terminated with a 50-Ω load. The switching of different modes of the ODPA is achieved by welding an 8.8-pF RF capacitor.

Fig. 21 shows the measured DE versus output power under a 50-Ω load at 2.1 GHz. The single-input case without the addition of a control signal is also plotted in the figure for comparison. The maximum power of the main RF input signal was set to 33 dBm, and the CSP was constant at 17 dBm, which is 16 dB lower than the maximum main RF input power. The phase of the control signal is swept from 0° to 360° in steps of 10°. In mode I (Fig. 21a), after the addition of the control signal, the DE of the designed ODPA increased by up to 8 PPs within the OBO range, and the saturated output power increased by 0.4 dB. The saturated output power is 44.6 dBm with a DE of 69.7%. The DE at 6-dB OBO is 60.8%. In mode II (Fig. 21b), after the addition of the control signal, the DE of the designed ODPA increased by up to 9 PPs within the OBO range, and the saturated output power increased by 0.2 dB. The saturated output power is 44.9 dBm with a DE of 67.0%. The DE at 6-dB OBO is 53.5%. In addition to the measured efficiency versus output power characteristics, the measured gain versus output power is illustrated in Fig. 22. In both modes, the small-signal gain is approximately 15 dB and the saturated gain is approximately 10 dB, demonstrating good agreement with the simulation results.

The operation of the designed ODPA under load mismatch conditions is also evaluated. Figs. 23 and 24 show the measured DE and output power of the designed ODPA in

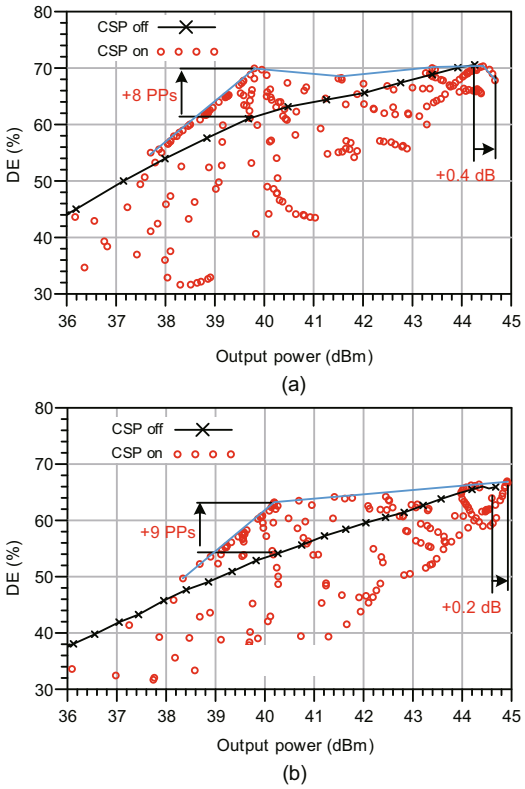

Fig. 21 Measured DE at 2.1 GHz: (a) mode I; (b) mode II

modes I and II, respectively, with a load mismatch VSWR of 2:1. The load impedances are marked in the Smith chart in each sub-figure. The CSP is constant at 20 dBm, and the other circuit parameters remain unchanged during the measurement. The measurement results demonstrate that compared with the simulation data, the results obtained from the two modes show obvious complementary characteristics. Modes I and II exhibit good efficiency performance under specific mismatch conditions, whereas performance deterioration is more obvious under inappropriate mismatch conditions. This may be because in the case of severe mismatch, the working state of the transistor significantly deviates from the normal operating region, which is very demanding for the transistor model used in the simulations and is more likely to deviate from the real-world behavior. Consequently, in some cases, the discrepancy

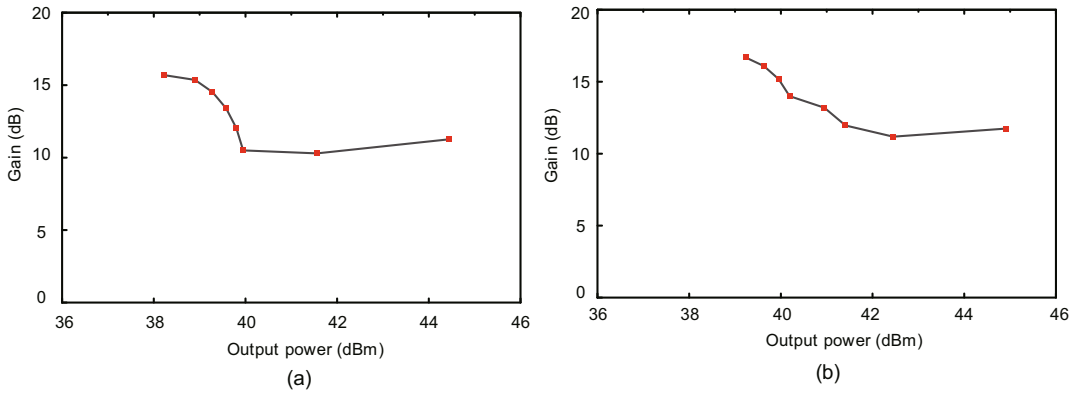

Fig. 22 Measured gain versus output power at 2.1 GHz: (a) mode I; (b) mode II

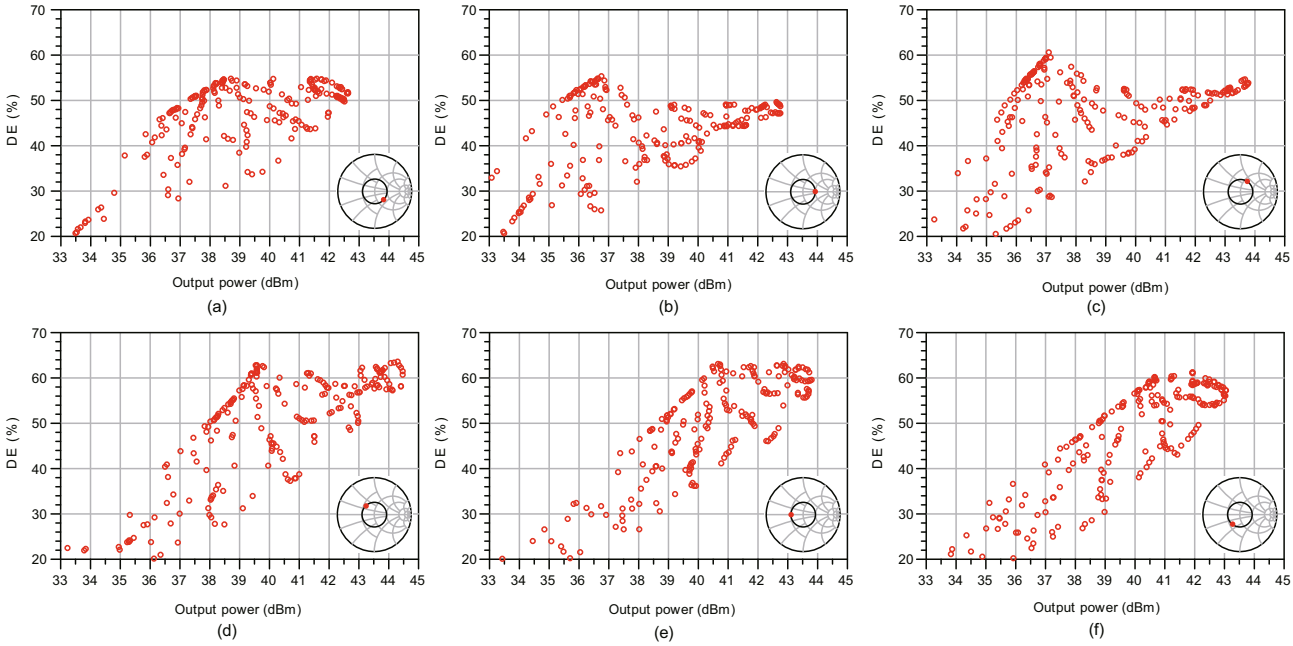

Fig. 23 Measured DE versus output power under 2:1 VSWR in mode I: (a) −60°; (b) 0°; (c) 60°; (d) 120°; (e) 180°; (f) 240°

between simulation and measured data becomes pronounced, particularly when the simulated performance already indicates degradation.

Fig. 25 illustrates the complementary characteristics of the two modes under various mismatch conditions. Fig. 25a shows the 6-dB OBO DE, and Fig. 25b shows the saturated DE and output power of the two modes under different mismatch load conditions. When the VSWR phase is in the range of −60° to 120°, mode I exhibits better OBO efficiency, whereas when the VSWR phase is in the range of 120° to 240°, mode II performs better. The saturated output power of the two modes is not significantly different. By combining the two modes, the designed ODPA can achieve a 6-dB OBO DE higher than 47.2% and saturated output power greater than 42.8 dBm under all load mismatch conditions with a VSWR of 2:1 in the simulations. Compared with the case of a 50-Ω load, the saturated output power is reduced by 2.1 dB at most.

Table 1 shows the performance comparison between this work and the recently published PAs. Among them, there are dual-input DPAs (Kalyan et al., 2019; Shi et al., 2023), quasi-balanced DPA (Lyu et al., 2021), and three-way DPA (Pang et al., 2024). It can be seen that the designed ODPA shows relatively high efficiency whether with a 50-Ω load or a mismatched load. In addition to the efficiency at the OBO point, the efficiency of the ODPA is further improved between the OBO point and the saturation point due to the injection of CSP and the modified OMN.

5 Conclusions

This study introduces a novel dual-input ODPA architecture. By introducing an orthogonal architecture with CSP injection and cooperating with a modified OMN, the efficiency of DPAs during the entire active load modulation process can be improved. The power of the control signal can be significantly lower than that of the main RF input, reducing the cost of the dual-input system. In addition, the proposed ODPA achieves dual-mode operation by leveraging reciprocal bias, resulting in high-efficiency operations under load mismatch conditions.

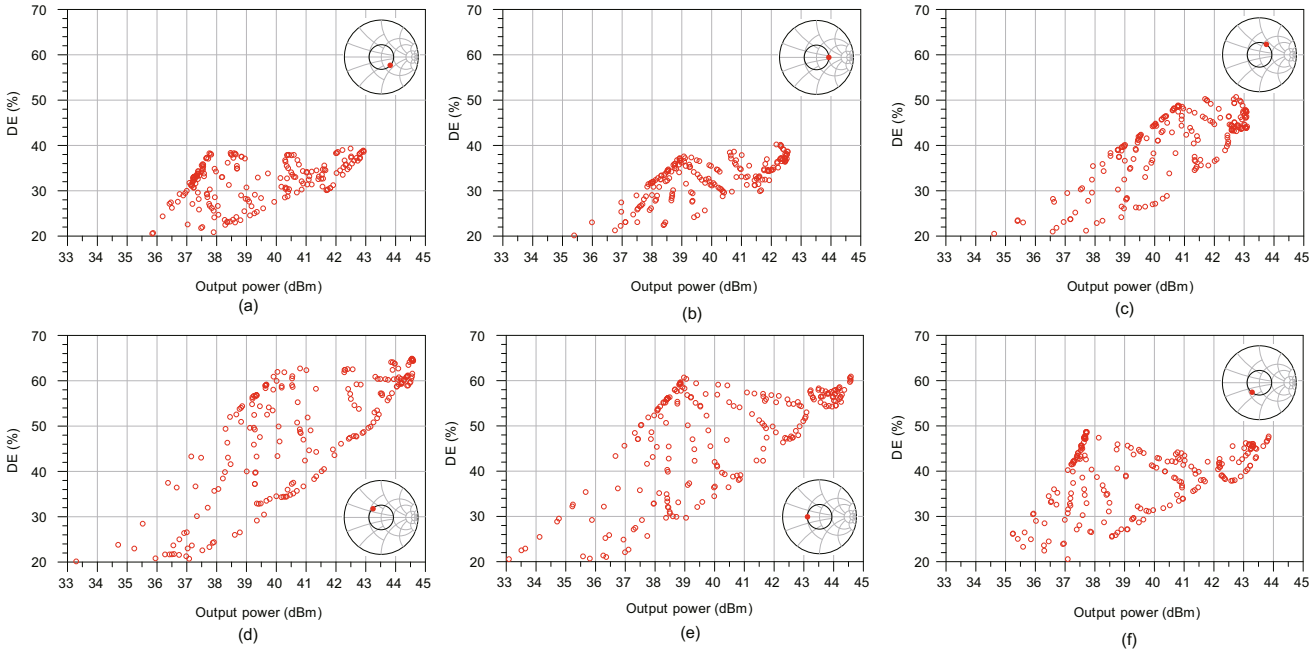

Fig. 24 Measured DE versus output power under 2:1 VSWR in mode II: (a) −60°; (b) 0°; (c) 60°; (d) 120°; (e) 180°; (f) 240°

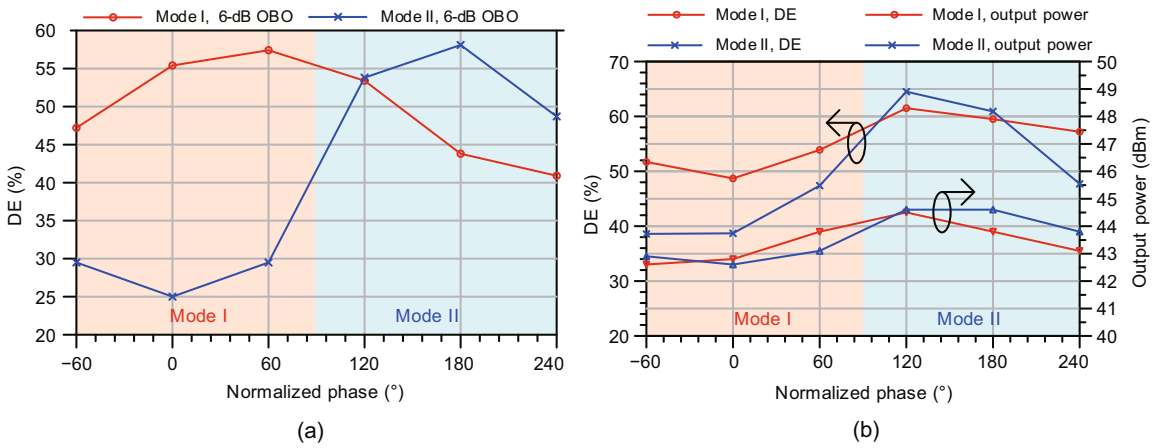

Fig. 25 Measurements under a 2:1 VSWR over the entire phase range: (a) DE at 6-dB OBO; (b) DE and output power at saturation

Table 1 Performance comparison of the recently published PAs

Reference	Frequency (GHz)	OBO (dB)	P_{sat} (dBm)		DE_{sat} (%)		DE@OBO (%)	
			Load=50 Ω	VSWR=2:1	Load=50 Ω	VSWR=2:1	Load=50 Ω	VSWR=2:1
This work	2.1	6	44.6/44.9	42.8–44.6	69.7/67	48.7–64.5	60.8/53.5	47.2–58.1
Kalyan et al. (2019)	3.6	6	44.2		68		65	
Lyu et al. (2021)	2	6	40.7	38.8–40.4	70.1	50–60*	59.8	Not mentioned
Shi et al. (2023)	3.5	6	43.4/43.7	41.5–43.3	69.1/70.8	52.8–60.7	>60	50.1–62.5
Pang et al. (2024)	2.0	9	46.4/46.7	44.8–46.3	70.3/72.2	50.2–65.8	62.8/60.7	47.8–56.7

* graphically estimated

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Author contributions

Yi JIN and Jingzhou PANG designed the research. Bingtao GAO and Ruibin GAO drafted the paper. Lei WANG, Jian LIU, and Mingyu LI helped organize the paper. Jingzhou PANG revised and finalized the paper.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Declaration on the use of generative AI tools

The authors declare that they have not used any generative AI tool during the preparation of this paper.

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